Matching Errors in MOSFET Current Mirrors

Good layout design is essential for circuits needed matched devices.

Layout techniques are effectively used to minimize first-order mismatch errors due to variations in these process parameters: gate-oxide thickness, lateral diffusion, oxide encroachment, and oxide charge density.

Considering only the effects of threshold voltage mismatch within the simple current mirror, its current ratio is described by

$$\frac{I_o}{I_{D1}} = \frac{b\left(V_{GS} - V_{THN} - 0.5\Delta V_{THN}\right)^2}{b\left(V_{GS} - V_{THN} + 0.5\Delta V_{THN}\right)^2} = \frac{\left[1 - \dfrac{\Delta V_{THN}}{2\left(V_{GS} - V_{THN}\right)}\right]^2}{\left[1 + \dfrac{\Delta V_{THN}}{2\left(V_{GS} - V_{THN}\right)}\right]^2}$$

$$\frac{I_o}{I_{D1}} \approx 1 - \frac{2\Delta V_{THN}}{\left(V_{GS} - V_{THN}\right)}$$

for SI saturation operation if a symmetric distribution in threshold voltage across the circuit is assumed (i.e., $V_{THN1} = V_{THN} - 0.5\Delta V_{THN}$ and $V_{THN2} = V_{THN} + 0.5\Delta V_{THN}$). Note the dependence on V_{GS}. A reduction in V_{GS} increases the input/output error in current mirrors induced by threshold voltage mismatch.

Considering only transconductance parameter mismatch,

$$\frac{I_o}{I_{D1}} \approx 1 + \frac{\Delta KP_n}{KP_n}$$

where the value of KP_n is the average transconductance parameter between the two transistors within the simple current mirror.

Considering only V_{DS} and λ effects,

$$\frac{I_o}{I_{D1}} = \frac{1 + \left(l_c + l_m\right)_2 V_{DS2}}{1 + \left(l_c + l_m\right)_1 V_{DS1}} \qquad \text{[SI sat.]}$$

These, too, can be a significant source of error (e.g., 11%! if V_{DS1} = 2V, V_{DS2} = 4V, $(\lambda_c + \lambda_m)_1 = 0.05\text{V}^{-1}$, and $(\lambda_c + \lambda_m)_1 = 0.04\text{V}^{-1}$).

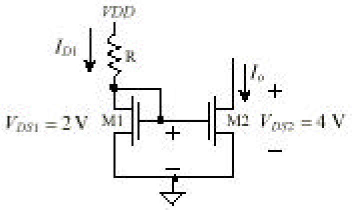


Figure 20.14 Basic current mirror with differing values of drain to source voltages.

Good layout practices for analog circuits include the following:

1) Use gate lengths several times larger than the technology's minimum gate length if all possible. This helps reduces λ effects while improving matching.
2) Use multiple source/drain contacts along the width of the transistor to reduce parasitic resistance and provides evenly distributed current through the device.

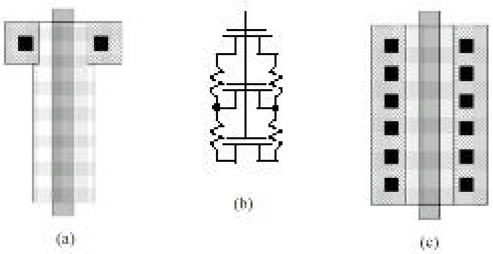


Figure 20.15 (a) Large device with a single contact and (b) its equivalent circuit. (c) Adding more contacts to reduce parasitic resistance.

3) Interdigitize large aspect ratio devices to reduce source/drain depletion capacitance. Using an even number (n) of gate fingers can reduce C_{db}, C_{sb} by one-half or $(n + 2)/2n$ depending on source/drain designation. Typically it is preferred to reduce drain capacitance more so than source capacitance. Also use dummy poly strips to minimize mismatch induced by etch undercutting during fab.

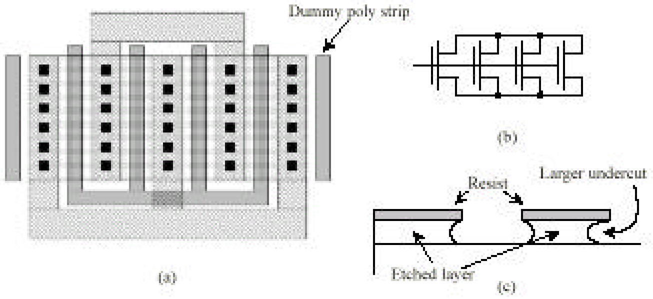


Figure 20.16 (a) A parallel device with dummy strips, (b) the equivalent circuit and (c) undercutting.

4) Matched devices should have identical orientation. An example of what **not** to do is shown below.

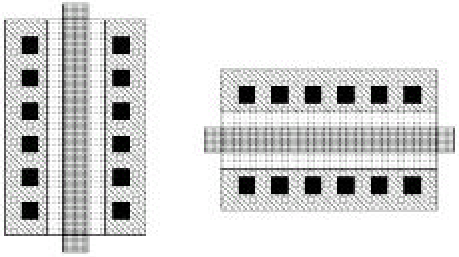


Figure 20.17 Devices with differing orientation.

5) Interdigitization can be used in a multiple transistor circuit layout to distribute process gradients across the circuit. This improves matching.

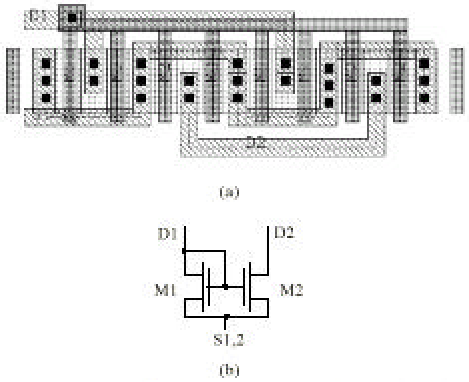


Figure 20.18 (a) Layout of a simple current mirror using interdigitation and (b) equivalent circuit.

6) Use **common-centroid** structures.

Other Current Sources/Sinks or Mirrors

Negative feedback is an effective technique for providing enhanced output impedance for current sources and sinks. Two circuits that demonstrate this are the Wilson current mirror and the regulated cascode.

Negative feedback action within the Wilson current sink ⇒ Suppose V_o increases while I_{D1} is constant. Then I_{D4} would increase causing V_{GS3} (= V_{GS2}) to increase which in turn tries to force I_{D2} to increase. But if I_{D1} is constant, then the voltage at node A must decrease since $I_{D2} = I_{D1}$ (V_{DS2} must decrease to accommodate increasing V_{GS2} while under constant current conditions). As a result, V_{GS4} would decrease, thus stabilizing I_{D4}.

The Wilson current sink's output resistance is given by

$$R_{out} = \frac{v_t}{i_t} = r_{o4}\left[1 + g_{m4}\left(r_{o3} \parallel \frac{1}{g_{m3}}\right)\left(1 + g_{m2}\left(r_{o1} \parallel r_{o2}\right)\right)\right] + g_{mb4}\left[\left(r_{o3} \parallel \frac{1}{g_{m3}}\right) + \frac{1}{r_{o4}}\left(r_{o3} \parallel \frac{1}{g_{m3}}\right)\right]$$

$$R_{out} \approx r_{o4}\left[1 + g_{m2}\left(r_{o1} \parallel r_{o2}\right) + g_{mb4}\left(\frac{1}{g_{m3}}\right) + \frac{1}{r_{o4} g_{m3}}\right]$$

$$R_{out} \approx r_o + g_{m2}\left(\frac{r_o^2}{2}\right)$$

The small-signal analysis for obtaining this result included the application of Ohm's Law (Eq. 20.42), KVL (Eq. 20.43), and KCL (Eq. 20.44).

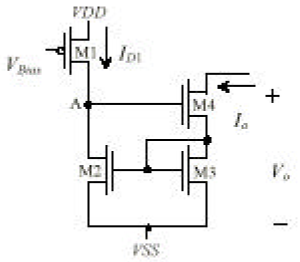


Figure 20.19 Wilson current mirror.

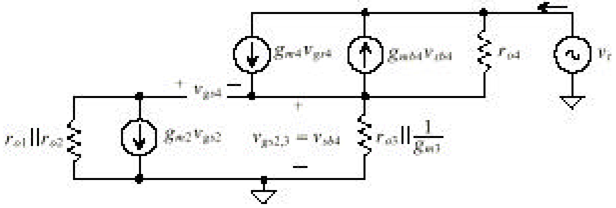


Figure 20.20 Small signal model of the Wilson current mirror used to determine output resistance.

The output voltage requirements for the Wilson current sink is described by

$$V_{o,\min} = V_{GS3} + V_{DS4,sat} = V_{GS3} + V_{GS4} - V_{THN4}$$

Alternately, in terms of output current,

$$V_{o,\min} = \sqrt{\frac{2I_o}{b_3}} + V_{THN3} + \sqrt{\frac{2I_o}{b_4}}$$

Hence, increasing I_o causes $V_{o,\min}$ to increase by twice the square root of I_o if $\beta_3 = \beta_4$. This is an unattractive characteristic of the Wilson current sink.

The regulated cascode current sink's negative feedback is as follows. Observe that V_{SG1} and V_{GS3} are constant (DC bias voltages). If I_o attempts to increase, the voltage at node A will rise, inducing an increase in I_{D2}. Then the voltage at node B must decrease since I_{D1} is constant. This reduction in V_{GS4} counters any increase in I_o. Subsequently, I_o is stabilized.

The regulated cascode current sink's output resistance is given by

$$R_{out} = \frac{v_t}{i_t} = r_{o4}\left[1 + g_{m4} r_{o3}\left(1 + g_{m2}\left(r_{o1} \parallel r_{o2}\right)\right) + g_{mb4} r_{o3} + \frac{r_{o3}}{r_{o4}}\right]$$

$$R_{out} \approx g_{m2} g_{m4}\left(r_{o1} \parallel r_{o2}\right) r_{o3} r_{o4} \approx \frac{g_m^2 r_o^3}{2}$$

10's of GΩ to 100's of GΩ of output resistance can be readily achieved!

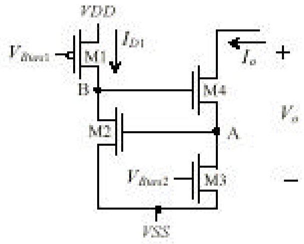


Figure 20.21 Regulated cascode current sink.

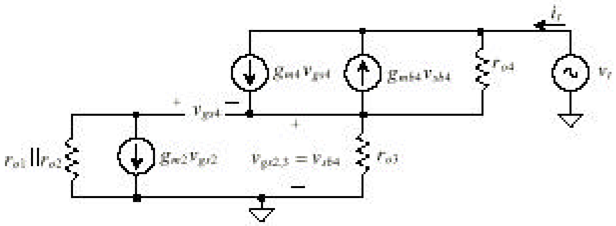


Figure 20.22 Small-signal model of the regulated cascode current mirror used to determine output resistance.

The output voltage requirement of the regulated cascode to maintain maximum output resistance is given by

$$V_{o,\min} = V_{GS2} + \left(V_{DS,sat}\right)_4$$

An example of a “simple” regulated cascode current mirror is shown below.

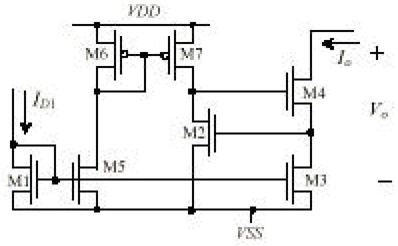


Figure 20.23 Regulated cascode current mirror.

Unfortunately, this implementation does not provide $V_{DS1} = V_{DS3}$, resulting in current mismatch.

The implementation shown below, however, provides improved current matching since (by design) $V_{DS1} = V_{DS3}$ (when all the transistors are matched).

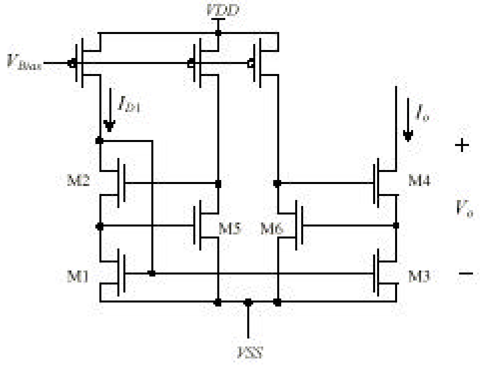


Figure 20.25 Improved regulated cascode current mirror.

The wide-swing cascode current mirror provides an output resistance of approximately $g_m r_o^2$ and an output voltage requirement of only $2V_{DS,sat}$ ($2\Delta V$).

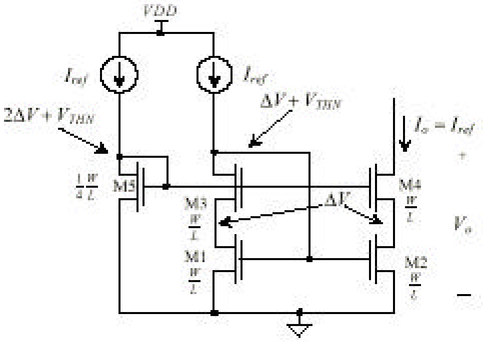
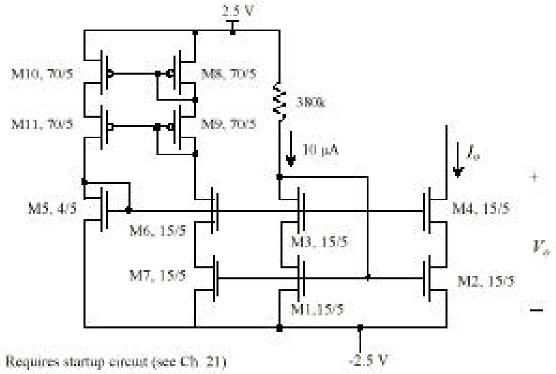


Figure 20.26 A high-swing cascode current mirror.

A practical implementation of this current mirror is shown below.



Requires startup circuit (see Ch. 21)

Figure 20.27 A 10 μA wide-swing current sink.

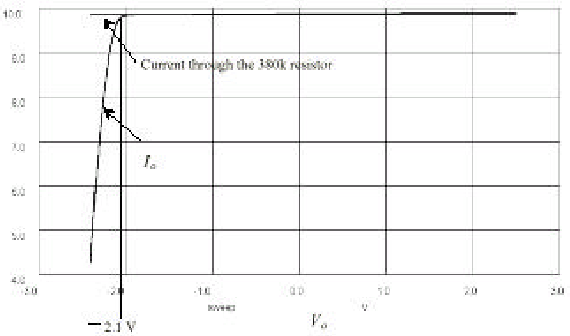


Figure 20.28 Simulation results for the current mirror of Fig. 20.27.