Active Gate Drive Solutions for Improving SiC JFET Switching Dynamics

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***Abstract*— Active and Non-Active Gate Drives (AGDs and NAGDs) are known for managing switching characteristics of silicon (Si) and silicon carbide (SiC) power semiconductors. As SiC adoption has grown, the need for intelligent gate drives which are capable of managing the dynamics associated with the fast-switching characteristics of these devices has become apparent. To propose a solution for managing driven and post-driven dynamic behavior, this paper first studies the most recent AGD solutions for silicon power semiconductors with focus on closed loop schemes. The study is continued by reviewing available AGD and NAGD solutions for silicon carbide power semiconductors concentrating on the SiC JFET. Oscillatory modes which can be observed in application circuits based on SiC devices are discussed, and an AGD design example is proposed for improving the final dynamic response of such circuits. The active gate drive design example is constructed, and both simulated and empirical results are shown to substantially reduce the occurrence of natural and forced oscillations at turn-off of the SiC JFET.**

I. INTRODUCTION

Gate drives can be divided into three categories: gate resistor control (standard drive), gate voltage control (voltage mode drive), and gate current control (current mode drive). Active Gate Drives (AGDs), which employ voltage/current mode configurations, achieve better control and thermal performance in comparison with traditional gate drives, which have considerable delays and losses. Recently proposed closed-loop and non-closed-loop AGDs for IGBT's have been published [1-17]. In Si power semiconductors, active gate drives are applied mainly to solve voltage/current imbalance and both driven and post-driven responses (forced and natural frequency oscillations). For multiple module designs, much research has been conducted on the voltage allocation problem in series IGBT applications and the current imbalance problem in parallel IGBT applications [18, 12-13]. For the application of discrete Si semiconductor switches, controlling di/dt during turn-on and controlling dv/dt during turn-off is the more common target of research. The authors of the current work are primarily interested in applying the concepts of those AGDs which are based on the use of compensated closed-loop control for the purpose of improving switching dynamics. The following references are examples of the AGD concept which are the focus of this paper. The current and voltage rates of change in a MOSFET are managed by means of a PI-compensated closed loop controller in [19]. In [20] the same issues for an IGBT are controlled by means of a closed loop control system, using an integrator compensator in the current loop. Control of the driven response is addressed by a phase lead compensator used in a closed-loop control system for an IGBT in [21]. It should be noted that the use of the term active gate drive (AGD) throughout this manuscript is intended to refer to the application of active compensation methods involving closed-loop control for the improvement of switching dynamics.

For SiC devices such as the SiC JFET, gate drive solutions range from the most recent non-active gate drives to a high bandwidth AGD. Non-active gate drives for the SiC JFET have had a considerable presence in the literature in recent years. For the cascode combination of a SiC JFET and Si MOSFET, older papers such as [22] propose a gate drive implemented by means of simple electronic components to guarantee high speed switching by limiting the gate-source voltage within a permissible range during the turn off process. The ADuM1233, a MOSFET/IGBT isolated half-bridge gate driver made by Analog Devices, is also used to drive normally-on SiC JFETs [23]. While some recent works improve or use available silicon driver IC's to implement gate drives [23-25], some other works even present their proposed IC gate drive [26]. Non-active gate drives have limited means to control the natural response of the power circuit, and what control is available usually limits dv/dt with the consequence of increasing the switching loss. A two-mode AGD is proposed for driving a half-bridge SiC JFET for a motor-drive

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application in [27-28]. The first mode is current-mode control, which manages the Miller plateau during the transient period. The second mode is voltage-mode control, which controls steady state operation. Adjustable current feedback delivers constant current during the Miller region transient; in parallel, drain voltage feedback is used to reduce the gate current during turn off to limit overvoltage. This AGD has been implemented by means of an operational amplifier and a BJT totem pole. The opportunity for an active JFET gate drive to improve both the driven (i.e., the dv/dt or Miller phase of the switching event) and the post-driven switching dynamics is a premise which finds ample support in the available literature.

II. Natural Response and Possibility of Sustained Oscillation

In this study, particular emphasis is placed on methods for arresting the occurrence of parasitic-induced oscillations during and after switching events in applications based on SiC unipolar devices. While the occurrence of parasitic-induced ringing is known in silicon-based applications [7], it is frequently more pronounced in SiC-based applications. This is due to the fact that SiC devices, and particularly SiC JFET's, are characterized by extremely low specific on-resistance and low intrinsic capacitance. These devices therefore switch very quickly and the switches contribute very little in the way of resistive damping to the power loop of the application. In the authors' experience, the lower the specific on-resistance of a particular device, the more likely it is to reveal parasitic-induced ringing when embedded in a power electronics application circuit.

In a recent work by the authors [29], a separate phenomenon was reported which is also related to the near-ideality of very low specific on-resistance devices. This phenomenon is the occurrence of sustained oscillations after the driven portion of the device turn-off event has concluded. Sustained oscillations are possible when there exist both non-negligible gate-loop inductance and non-negligible drain-loop inductance. During the turn-off dv/dt event, displacement current flows through the Miller capacitance, and energy is stored in the gate loop inductance, which causes the gate-source voltage to swing below the negative gate drive voltage rail after turnoff. This under-shoot then causes the gate-source voltage to ring back above the negative rail voltage. If ring-back to threshold occurs, then the device may turn back on and recharge the drain-loop parasitic inductance, which creates the initial conditions necessary for another cycle to occur. Depending on the values of the parasitic inductances in the circuit and the intrinsic capacitances and transconductance of the switch, it is possible for this pattern to develop into a sustained envelope of oscillations which continues until the bus is depleted of energy, the switch is actively gated on, or the switch is destroyed. An example of this sustained oscillation phenomenon for a SiC JFET is shown in Fig. l. This phenomenon has also been recently referenced as a known risk both for SiC MOSFET's [30] and enhancement-mode GaN FET's [31]. These devices all share the risk of sustained oscillation due to their inherent fast-switching characteristics and lack of contribution to power-loop damping.

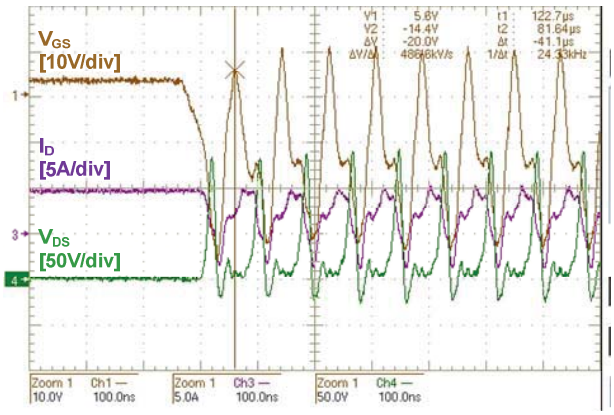


Figure 2: Example of Sustained Oscillation for SiC JFET; the brown waveform is gate-source voltage; the green waveform is drain-source voltage; and the purple waveform is drain current.

III. AGD for Improving SiC JFET Natural Response

As part of this work, a simulation study was carried out to determine the feasibility of mitigating the oscillatory modes described in Section II through the application of an active gate drive circuit. First, a manufacturer-supplied LTSpice model of the SemiSouth SJEP120R100 SiC JFET was utilized to evaluate whether the natural and sustained oscillation phenomena could be observed in time-domain simulation. This model was able to demonstrate both the parasitic-induced natural ring-down and the sustained oscillation condition when operated under conditions similar to those which are known to produce these modes in real devices. Specifically, the conditions necessary for the sustained oscillation to occur include the insertion of a non-negligible amount of gate-loop and drain-loop inductance. The inductance values used in simulation are far above what would be expected for a well-designed high-power-density converter, but not unrealistic for applications requiring cabling such as that described in [7]. Next, a reduced-order dynamic model of the SiC JFET and the traditional open-loop gate-drive circuit was created and subjected to frequency-domain analysis (Fig. 2). This small-signal model utilizes a simplified parasitic representation of the SiC JFET in the cut-off condition, and the intrinsic

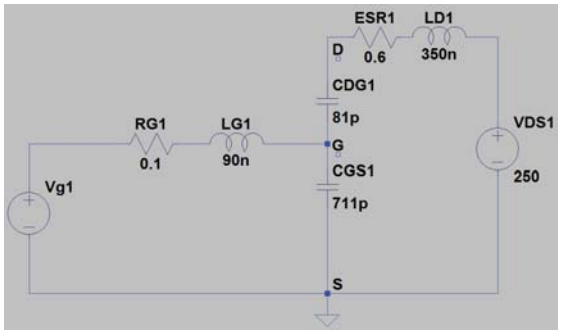


Figure 1: Reduced-order SiC JFET dynamic model and open loop gate drive

capacitances are linearized around a bus voltage of 250 V. The result of this analysis demonstrated that there is an opportunity for an active gate drive which improves the dynamic behavior of the JFET-based circuit during switching. Section IV presents a design example of a potential AGD intended to accomplish these objectives.

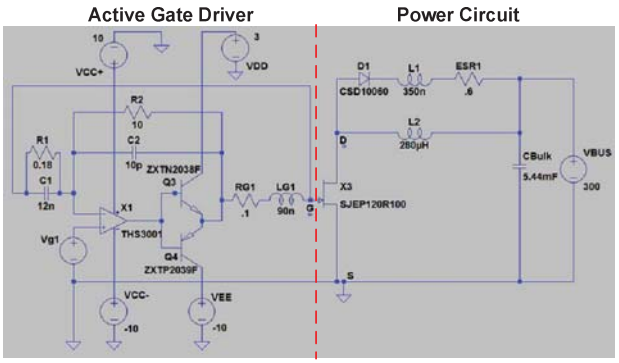
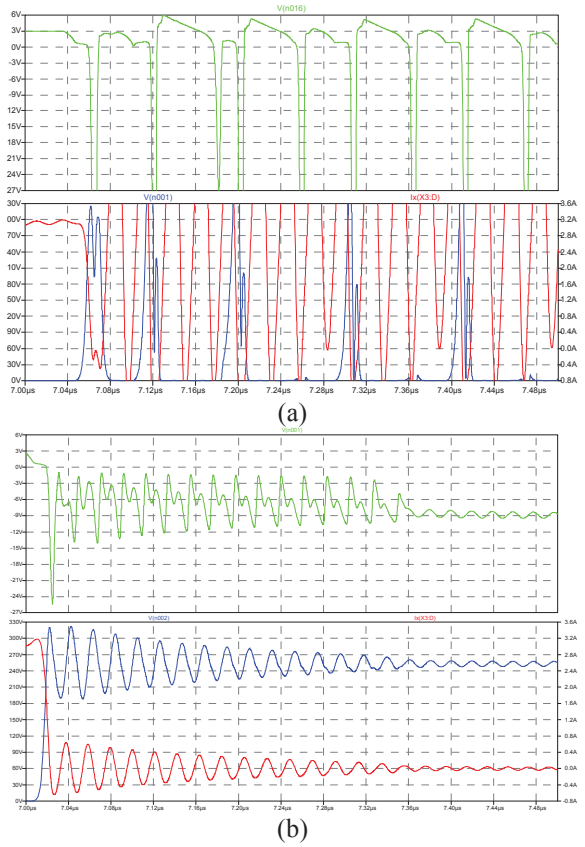


Figure 4: Proposed SiC JFET Active Gate Drive and Power Circuit



(a)

(b)

Figure 3: Simulation results for simplified dynamic model after turn-off. Subplot (a) is the uncompensated response; Subplot (b) includes the effect of AGD compensation. The green trace is gate-source voltage (10V/div); the blue trace is drain-source voltage (30V/div); the red trace is drain-source current (0.4A/div)

IV. Design

The closed-loop silicon AGD solutions and the SiC JFET AGD embodiments surveyed in Section I encourage the design of a closed-loop SiC AGD to arrest the natural and forced oscillatory modes described in Section II. One design example selected for use in this work is depicted in Fig 3. A high-frequency and high-slew-rate operational amplifier and a high-frequency BJT totem pole were selected to provide sufficient bandwidth to enable this AGD to respond to the oscillatory modes described in Section II. This active gate drive employs a closed loop negative feedback system to provide gate voltage mode control. State space equations and frequency analysis of the circuit shown in Fig. 2 were used to design the compensator for this AGD. Standard component values were selected to be as close as possible to the calculated values obtained from frequency-domain analysis. The introduction of this AGD into the time-domain simulation described in Section III resulted in a reduction in the severity of both natural, parasitic-induced ring-down as well as the phenomenon of sustained oscillations. Simulation results showing the behavior of the test circuit both before and after the introduction of the AGD are demonstrated in Fig. 4. These results indicate that the proposed AGD design could potentially reduce the susceptibility of a SiC-based design to these oscillatory phenomena.

V. Empirical Study

As part of this work, the AGD design described in the previous section was constructed and attached to a power circuit. The 1" by 1" AGD PCB and its attachment to the power circuit are shown in Figure 5. For these experiments, a single SemiSouth SJEP120R100 SiC JFET was used to switch a clamped inductive load at a constant drain current. The bus voltage for these experiments was varied from 200 V

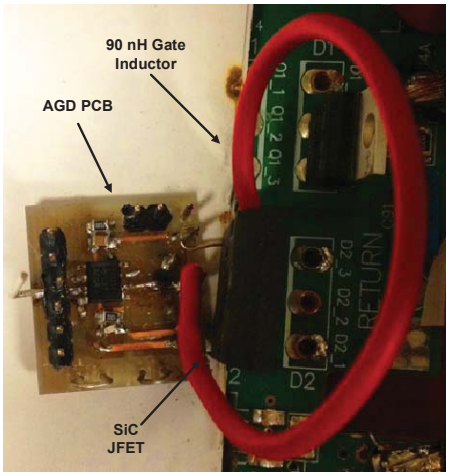
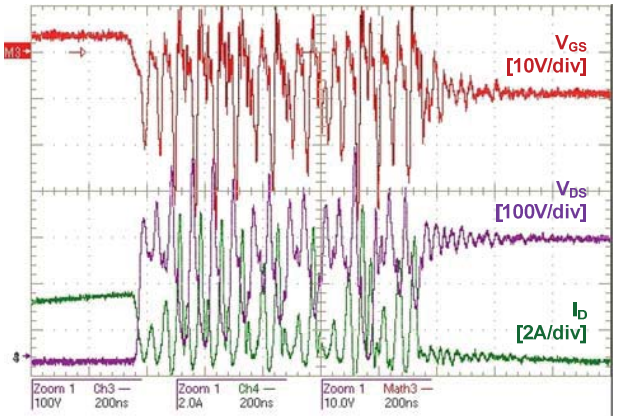
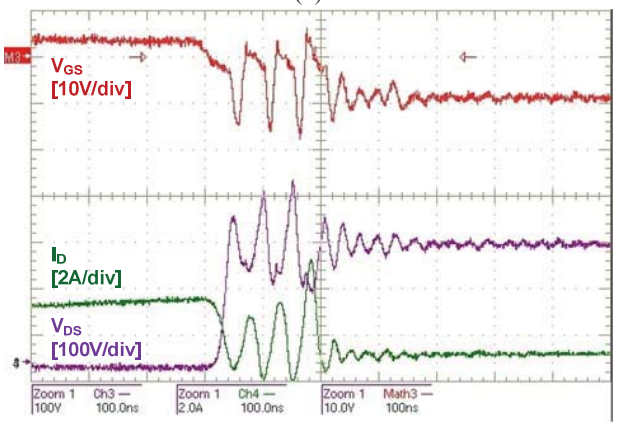


Figure 5: AGD Implementation and Attachment to Power Circuit for Evaluation



(a)



(b)

Figure 6: Empirical test results for (a) uncompensated gate drive, and (b) compensated gate drive. The red trace is gate-source voltage; the purple trace is drain-source voltage; the green trace is drain current.

to 400 V in 25 V increments. This range of bus voltages demonstrated susceptibility to sustained oscillation with the levels of parasitic gate-loop and drain-loop inductance which were introduced into the circuit. A constant drain current of 2.8 A was selected in order to provide a moderate propensity for oscillation without introducing a significant risk of device destruction if sustained oscillations were to occur. For each represented bus voltage, the SiC JFET was switched both with and without the effect of the AGD included. Exemplary results from this test procedure at a bus voltage of 250 V are shown in Figure 6. Under the operating conditions depicted in this figure, the uncompensated design experiences a total of 16 oscillations, while the compensated design experiences only 3 oscillations. This result suggests that the proposed AGD design can provide a significant stabilizing influence for a circuit which contains significant parasitic inductance. Although the compensator is not able to arrest all oscillations, it nevertheless reduces the severity and duration of the sustained oscillation phenomenon. Figure 7 shows a summary of all empirical results obtained during this work in histogram format. In this figure, the number of oscillations observed for both the un-compensated and compensated cases

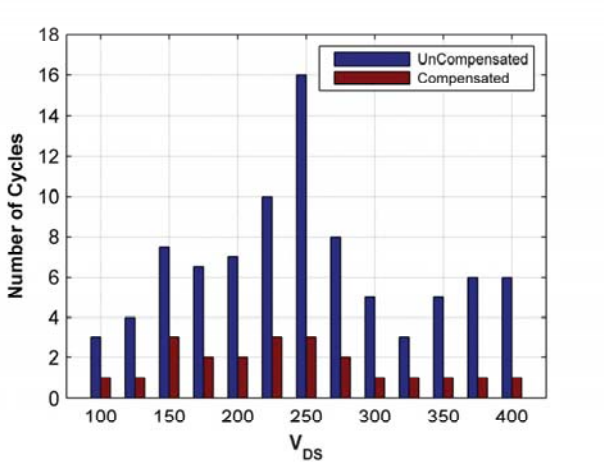


Figure 7: Summary of empirical results; Histogram of uncompensated design is shown in blue; Histogram of compensated design is shown in red.

are plotted together for comparison. It is apparent from this figure that the occurrence of forced oscillations is substantially reduced across all operating points by the introduction of the AGD compensator. In fact, the compensated design allows a maximum of three oscillations across the entire test set, while the uncompensated case was observed to experience as many as 16 oscillations. At a bus voltage of 250 V, the sharp increase in the number of oscillatory cycles observed in the uncompensated case represents a propensity for forced oscillation which did result in sustained oscillation and device destruction when the drain current was increased slightly to 5 A. But at all drain currents experimentally tested up to 5 A the AGD-compensated design arrested the forced oscillations and allowed the device to complete the turn-off transition safely.

VI. Conclusion

This paper provided a survey of the most recent Si AGDs, with focus on closed loop options, and both active and non-active gate drive solutions available for SiC unipolar devices. This literature review motivated a closer investigation into the possibility of implementing a closed-loop active gate drive for the SiC JFET to arrest the occurrence of both natural and forced oscillations at turn-off. An exemplary closed-loop AGD design for the SiC JFET is proposed, and this design is subjected to simulation as well as empirical analysis. The results of this study indicate a substantial improvement of the switching characteristics of the controlled device at turn-off. The susceptibility of the application circuit to sustained oscillations was dramatically reduced, and the stress on the gate-source junction was reduced as well. Emphasis in the reference design was placed on selecting components and analyzing the plant model so as to include the natural frequency of the application circuit within the control bandwidth. This approach is unique in the literature reviewed to date.

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