Stable High dV/dt Switching of SiC JFETs Using Simple Drive Methods

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Abstract— **Due to low on-resistance and low intrinsic capacitance the SiC JFET is capable of very high dV/dt in principle. However, these advantages often result in the excitation of resonant modes during switching. The low on on-resistance of the device results in less contributes little damping of to the L-C resonance in the circuit. Under conditions which are realizable in applications, the devices will manifest sustained oscillations. Typically these problems are addressed by reducing the switching speeds using various dissipative methods. These methods focus on symptomatic effects rather than causes. Careful consideration to parasitic inductances in circuit layout can yield very high dV/dt switching (e.g. > 30 V/ns) with only the need for modest series gate resistance to achieve stable operation. This paper demonstrates this effect experimentally, reporting the highest known switching rates of inductive currents for these devices to date.**

I. INTRODUCTION

Commercially available silicon carbide (SiC) transistors have penetrated a growing number of applications in power electronics. Cost versus performance has reached levels allowing economically competitive designs using SiC devices. Due to low on-resistance and low intrinsic capacitance SiC unipolar devices can switch at very high rate. However, also due to these characteristics a high-rate switch has the potential to excite resonant modes in the system. This effect is most often seen as damped oscillations in both the gate and power loops [1-3]. This ringing can result in increased switching losses in the system as well as pose issues of electromagnetic interference (EMI). A related yet more problematic effect is the occurrence of self-sustaining oscillations at turn-off. This problem has been observed in SiC devices by the authors, studies of which are reported in [4, 5]. The following is reported in a datasheet for a recently released half-bridge silicon carbide MOSFET module," The interconnection between the gate driver and module housing needs to be as short as possible. This will afford the best switching time and avoid the potential for device oscillation. [6]" At present, most designs fall short of full utilization of SiC device capabilities often due to the need to mitigate the phenomena described. This is typically achieved through the reduction of dV/dt to levels that reduce the capacity of the circuit to excite resonant modes. Most commonly this is realized either through the addition of large series gate impedances, additional gate-source capacitance, or the incorporation of snubbing elements, all of which are undesirable or non-optimal and result in increased power dissipation, increased part count, and higher cost. Each of these techniques addresses the symptoms of this problem rather than the cause. In principle, achievement of high dV/dt low energy switching is not due to device limitations limited solely by device characteristics, but is convolved with circuit design and layout. A gate driver has been developed with low parasitic gate inductance for the SiC depletion mode JFET. It is shown experimentally that turn off stability can be is dependent upon series gate impedance. Reduction of gate inductance can enable stable gate drive with minimal additional gate resistance and as a result high dV/dt switching (e.g. > 30 V/ns) can be achieved.

II. SWITCHING, THE NATURAL RESPONSE, AND INSTABILITY

Fig. 1 shows a generalized clamped inductively loaded circuit and a notional driver. This generalized circuit shows all of the circuit elements including parasitics which lead to both ringing due to the natural response as well as the special case of sustained oscillations. It should be noted that all of the elements in this circuit are inherent to unipolar devices

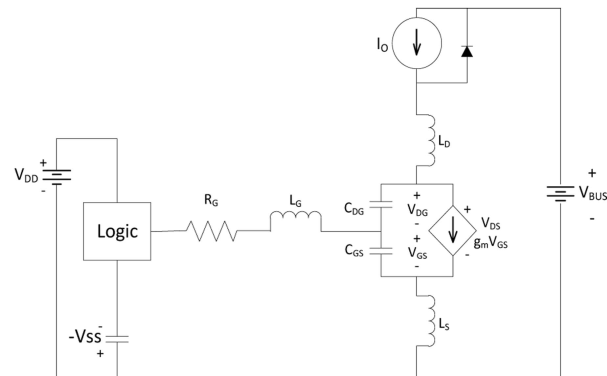

Figure 1. Stable device Turn-off at dV/dt = 32 V/ns *Channel 3 (purple) – Drain Current [5 A/div], Channel 4 (green) – Drain-Source Voltage [200 V/div]*

thus all devices are susceptible in principle to this phenomenon under the proper conditions. Much literature is available observing the natural response of the gate-source voltage at turn-off [1-3,7-13]. This is normally observed as damped L-C resonant voltage at the gate-source terminal interface, as well as in the bus voltage as shown in Fig. 2. Under some conditions the natural response can result in the gate-source voltage ringing back to the threshold voltage thus modulating the channel current which can produce sustained oscillations as shown in Fig. 3. Arresting this issue is typically achieved via application of additional gate-source capacitance or series gate resistance. The primary cause of ringing in the natural response and forced oscillations is L-C resonance between equivalent series inductance in the application circuit and the switch capacitance. Further, due to the non-linearity of the Miller capacitance both the natural response and sustained oscillations are dependent upon drain-source voltage. As a result stable operation can be observed at higher voltages approaching the device voltage rating however instability may still occur over a window of operating points far below the device ratings. For example, dV/dt measurements as high as 44 V/ns have been observed at the voltage and current limits of this study (Vds = 600 V, Id = 20 A); however, stable switching was not achievable at lower input voltages. The phenomenon of the drain-source voltage creating a susceptibility envelope to oscillation is understood to be due to the non-linearity of the Miller capacitance. Given that susceptibility to sustained oscillations is a product of switching speed, inherent device characteristics, and application parasitics, the reduction of parasitic reactive elements is a required condition for the simultaneous achievement of stability and high dV/dt. Since the operable capacitance is intrinsic to the device, circuit designers have little leverage for manipulating capacitance to quell the natural response. However, if careful consideration to parasitic inductance is given during system layout, susceptibility to LC resonance can be greatly reduced. By minimizing series gate inductance the capability of the gate drive to inject gate charge at a high rate to achieve stable switching at high dV/dt is possible. Simple drive circuits can be sued with low series gate resistance with adequate minimization of series gate inductance.

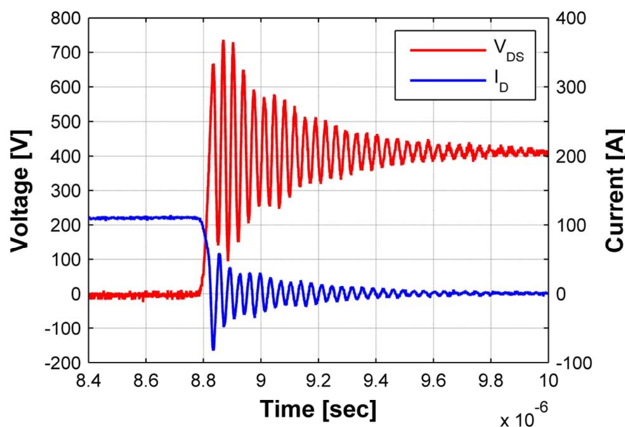

Figure 2. The Natural Response at Turn-off

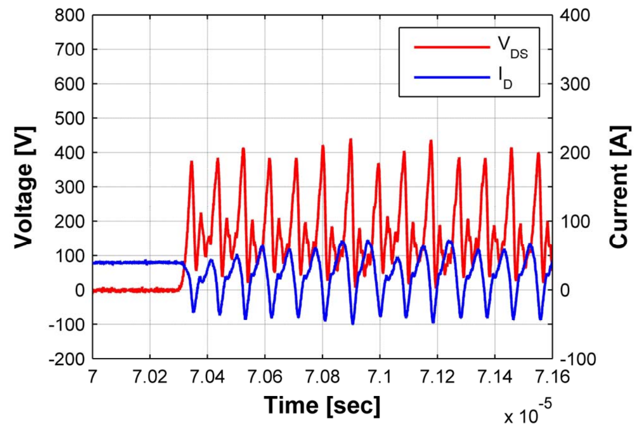

Figure 3. Sustained Oscillation at Turn-off

III. EXPERIMENTAL RESULTS

A clamped inductively loaded (CIL) circuit based on these principles was constructed. A low impedance totem pole gate drive was integrated with the CIL circuit. A SJDP120R045 SiC JFET from Semisouth Laboratories was used as the switching element and a SiC Schottky barrier diode was used to passively clamp the inductive load current. Evaluations of switching performance were recorded using the double pulse method for drain currents up to 20 A and an input voltage that was varied from a low of 10 V and a high of 600 V in 10 V incremental steps. Series gate resistance values in steps from 0.1 Ω up to 5 Ω were evaluated. Drain-source voltage dV/dt at turn-off was measured for each combination where stability was achieved for all voltages up to an input voltage of 600 V. Table 1 shows drain-source dV/dt measurements for varied gate resistance at a drain-source voltage of 600 V and drain current of 20 A. Instability is noted for any series gate resistance selection which resulted in any unstable switching across the evaluated envelope of drain-source voltages. Unstable as listed in Table 1 does not indicate that switching instability was observed at high drain-source voltages. A typical switching measurement for this test is shown in Fig. 4. A minimum value for stable operation can easily be established via this empirical method.

TABLE I. SERIES GATE RESISTANCE AND DRAIN-SOURCE DV/DT

R_g [Ω]	dv/dt [V/ns]
0.1	Unstable
0.5	Unstable
1.0	32.7
2.0	25.4
3.0	20.9
3.9	17.8
5.1	15.0

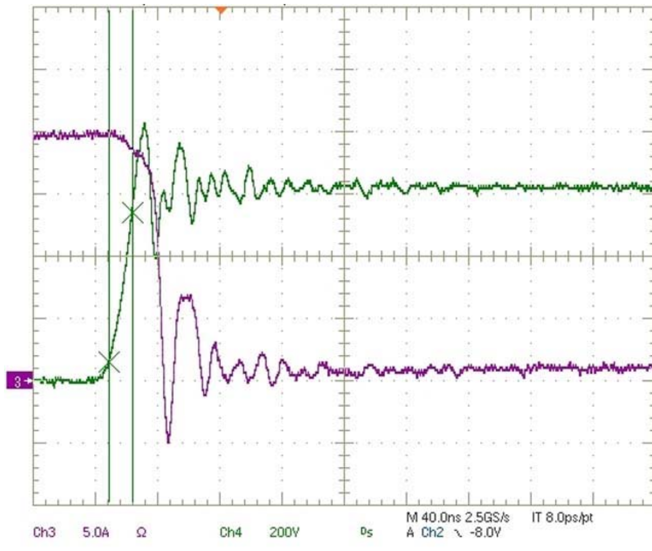

Figure 4. Stable device Turn-off at dV/dt = 32 V/ns, *Channel 3 (purple) – Drain Current [5 A/div], Channel 4 (green) – Drain-Source Voltage [200 V/div]*

As expected Table 1 demonstrates a reduction in dV/dt as series gate resistance is increased. Very high dV/dt can be achieved using the SiC JFET simply through proper gate drive layout. The non-linearity of the device capacitance results in the greatest region of instability for the devices in this experiment at voltages between 50 V and 200 V. This is due to the decreasing ratio of gate-drain (Miller) capacitance to gate-source capacitance as described in the previous section (an analytical treatment which explains this observation is found in [4]).

IV. CONCLUSIONS

The silicon carbide JFET is capable of safely switching inductive currents at very high dV/dt. This paper has documented the highest stable switching speeds yet recorded for these devices. Careful design can minimize parasitic inductances resulting in the need for only modest series gate resistance to eliminate forced oscillations and sufficiently damp the natural response of the gate-source voltage. Given the inherently low gate-source and Miller capacitance of the SiC JFET, gate drive requirements are similarly modest. Sophisticated gate drive topologies are not necessary to achieve these results. Further work is required to accurately model switching dynamics. Continuing the study of the cause of sustained forced oscillations of the device could yield even higher switching speeds and lower switching energies.

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