Gate-Drive Considerations for Silicon Carbide FET-Based Half-Bridge Circuits

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Abstract

Silicon Carbide field-effect devices are known to enable high-performance power electronics applications due to their low intrinsic capacitance and low specific on-resistance. However, non-negligible oscillatory phenomena, including instability, can accompany this increased performance, particularly in applications based on the half-bridge topology. This paper presents an analysis which enables designers to ensure the stability of applications based on this topology through careful management of gate-drive loop impedance.

1. Introduction

The recent introduction of commercially available wide band-gap field-effect transistors has led to a growing adoption of these devices in commercial power electronics applications. In some cases, the achievement of high efficiency and low losses in these systems has been accompanied by an unexpected increase in observable oscillatory modes when compared to silicon-based systems, especially in applications based on the half-bridge topology. This can happen because SiC devices have lower specific on-resistance and lower intrinsic capacitance than comparable silicon devices. As a result, these devices switch quickly and contribute little resistive damping to the power loop of the attached application circuit. The resulting poor dynamics of such systems have been studied in many papers such as [1]-[2]. In some cases, the poor dynamics present in these systems can lead to the occurrence of half-bridge instability, which is distinct from the damped natural LC-resonance commonly observed in high-speed switching circuits. In a previous work by the authors, the instability phenomenon has been given a full analytical treatment in the form of the negative resistance model commonly used to describe the design of linear oscillators [3]. In this work, the treatment established previously is used to provide specific recommendations regarding the gate-drive design needed to ensure stability of half-bridge circuits while maximizing switching speed.

2. Analysis of Self-Sustained Oscillation

An exemplary inductively-loaded switching test circuit used to provide the necessary framework for the current treatment is shown in Fig. 1. In this circuit, Q_1 is not actively switched but is biased in the off-state; Q_2 is actively switched using the double-pulse test method; and the inductive load is represented as a current source. Under conditions which will be described later in this paper, it is possible to observe self-sustained oscillation of this circuit when Q_2 is switched off. Fig. 2 demonstrates this condition for a half-bridge composed of 1200 V depletion-mode SiC JFET's. In this example, Q_2 is observed to oscillate in a self-sustained manner at approximately 12.5 MHz.

A full explanation of the theory describing this self-sustained oscillation phenomenon is available in another work by the authors [3]. However, for the purpose of establishing context for the current work, a brief synopsis is presented here. In order to understand this phenomenon, two resonant tank circuits must be considered. The first resonant tank is the gate-loop tank which is made up of the parasitic gate-loop inductance (L_{G2}) and the input capacitance of Q_2. The second resonant tank is the drain-loop tank which comprises the parasitic drain-loop inductance (L_D) and the output capacitance of Q_2 (applicable at the turn-off of Q_2).

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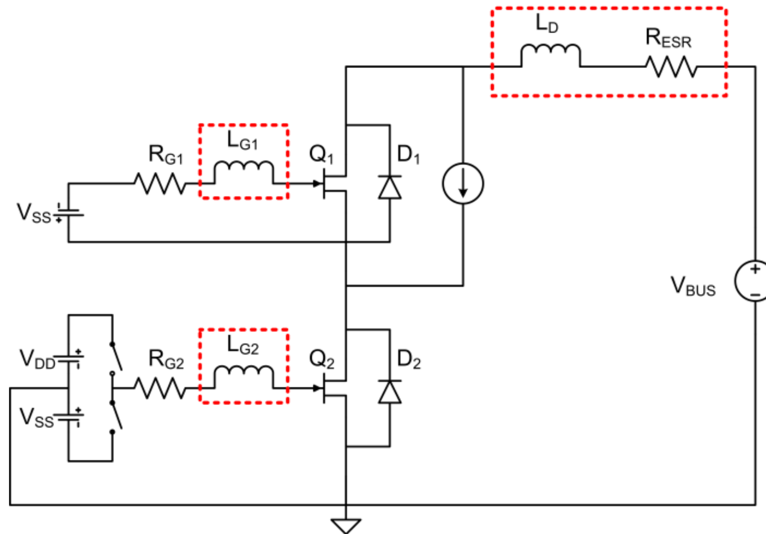

Fig. 1. Half-bridge-based CIL test circuit used to describe instability phenomenon. Parasitic elements are outlined with red dashed boxes. Note that the top switch is not actively gated, but is biased OFF. The clamped inductor is represented as a current source.

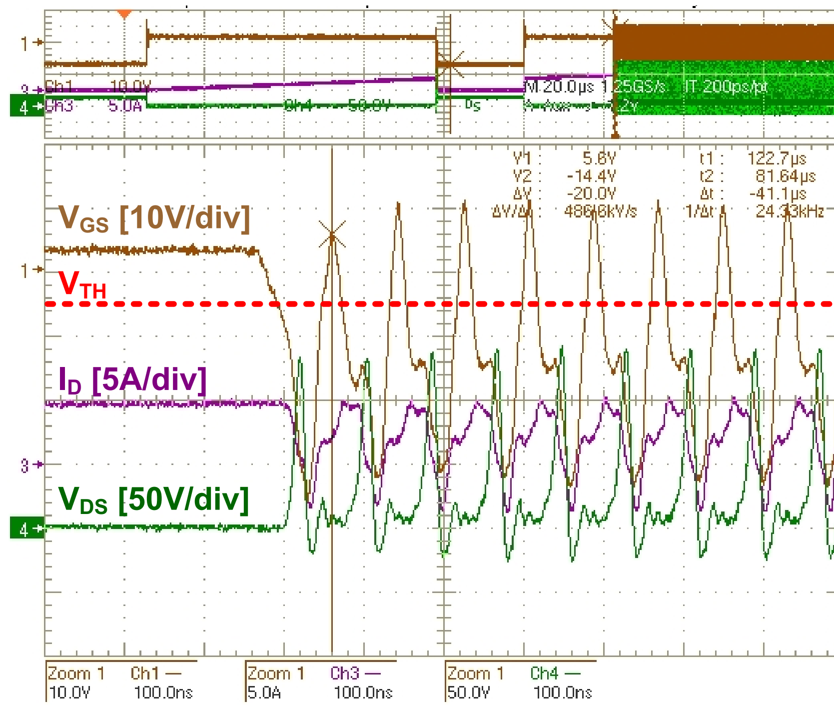

Fig. 2. Turn-off waveforms for a SiC JFET half-bridge demonstrating self-sustained oscillation. Note the constant oscillation envelope evident in the upper zoom window. The brown trace is gate-source voltage; the purple trace is drain current; the green trace is drain-source voltage.

When the active switch (Q_2) is gated off, energy is stored in the gate-loop inductance (L_{G2}). After the device channel is pinched off, this stored energy must be dissipated through a natural ring-down of the gate-loop resonant tank. If sufficient energy is stored in the gate-loop inductance, the gate-source voltage may rise to the threshold voltage during the first positive half-cycle of gate-loop ringing. This condition is evident in the first cycle of oscillation in Fig.

2. When the gate-source voltage rings back to threshold, Q_2's channel begins to conduct and this event influences the behavior of the drain-loop resonant tank. Ordinarily, the drain-loop tank rings down in a nearly second-order manner after Q_2 turn-off as the energy stored in this tank is dissipated in R_{ESR}. However, when the un-commanded channel conduction of Q_2 occurs, the current in L_D increases and energy is added back to the drain-loop resonant tank from the DC source. As a result, the amplitude of the drain-loop oscillation may be restored to the value attained in the previous cycle. In this way, the un-commanded channel conduction of Q_2 can be shown to enable the conditions necessary for self-sustained oscillation to occur.

An analytical framework capable of predicting the conditions under which self-sustained oscillation is likely to occur is established by casting the power circuit of Fig. 1 as a negative-resistance oscillator. This formulation provides a convenient means by which susceptibility to self-sustained oscillation can be evaluated in terms of energy balance, rather than through time-domain circuit analysis. This procedure makes use of the small-signal model shown in Fig. 3.

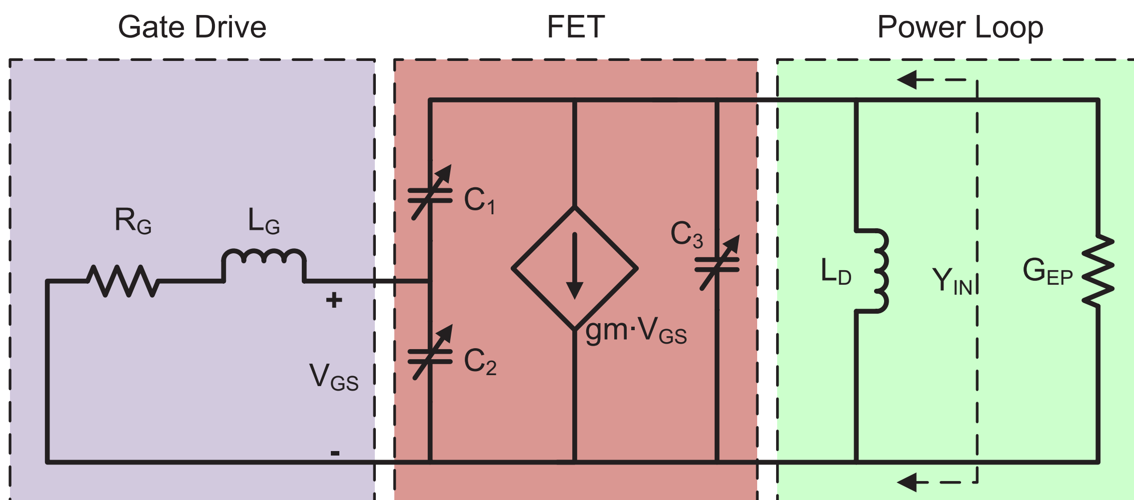

Fig. 3. Small-signal model of power circuit useful for determining risk of self-sustained oscillation

This small signal model is constructed from the CIL power circuit of Fig. 1 by eliminating independent current and voltage sources, and reflecting the power loop parasitic components as parallel equivalents, and assuming that $\omega L_D >> R_{ESR}$. In addition, the high-side switch is represented as a short circuit since it is effectively shorted out by forward-biased diode D_1 when switch Q_2 is turned off. In the previous work, a special case of the small signal model which omitted C_3 was used; this special case is applicable to devices without appreciable drain-source capacitance such as the vertical-channel SiC JFET. Here, a generalized formulation of this model is presented which is valid for any field-effect device.

As has been shown in [3], the susceptibility to self-sustained oscillation can be predicted by considering the admittance cut labelled Y_1 in Fig. 3. Due to un-commanded channel conduction of Q_2, the real part of Y_1 can be visualized as contributing negative resistance to the application circuit which counter-balances the dissipation resulting from the action of positive conductance G_{EP}. The magnitude of this negative resistance is the primary factor which influences whether the application circuit will experience self-sustained oscillation. Thus, if $Re\{Y_{IN}\}/G_{EP} \leq -1$, the model predicts the occurrence of self-sustained oscillation such as that shown in Fig. 2. On the other hand, if $Re\{Y_{IN}\}/G_{EP} > -1$, the model predicts the occurrence of self-extinguishing oscillation.

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Due to the nonlinear dependence of the FET intrinsic capacitances on the drain-source voltage, the resonant frequency of the circuit in Fig. 3 varies as a function of the bus voltage being switched by Q_2. As a result, the susceptibility to self-sustained oscillation is also dependent on the bus voltage. Constructing a plot of the quantity $Re\{Y_{IN}\}/G_{EP}$ as a function of bus voltage provides a means for quickly determining the susceptibility of a circuit to self-sustained oscillation. If the normalized conductance curve intersects or falls below the -1 point on the ordinate, then the circuit is at risk of self-sustained oscillation. If all points on the normalized conductance curve lie at values more positive than -1 on the ordinate, then the circuit is not expected to experience self-sustained oscillation at any drain-source voltage. This model has been shown to provide quantitative agreement to empirical stability results in [3].

3. Parameters of Sensitivity

For the purposes of the current work, it is desirable to understand the model parameters which most heavily influence the susceptibility to self-sustained oscillation. In particular, the effect of the components in the gate-loop is of primary interest, since the gate-drive circuit accounts for several important degrees of freedom available to the designer. Throughout the analysis in this section, separate consideration is given to SiC field-effect devices with negligible drain-source capacitance (such as the vertical-channel SiC JFET), and to SiC field-effect devices with non-negligible drain-source capacitance (such as the lateral-channel SiC DMOSFET). This latter case is also applicable to the configuration of a vertical-channel SiC JFET with an anti-parallel rectifier, which contributes an effective drain-source capacitance.

3.1. Series Gate Impedance

The first and most obvious parameter of sensitivity is the gate-loop series impedance. While good design practice involves minimizing the amount of parasitic inductance in the gate loop, it is not possible to completely eliminate this inductance. Furthermore, a recent publication at PCIM argues that 100-150 nH is a typical value of gate inductance in many applications (while further arguing that it should be reduced) [4]. The other component of the gate-loop series impedance is the gate resistor, R_G. In many designs, the value of this component represents one of the most important degrees of freedom available to the designer. While this value is generally chosen to satisfy several competing goals, the occurrence of instability in the gate drive circuit may not be a constraint considered by all application designers. With SiC or GaN field-effect devices, the low intrinsic capacitance makes this constraint an important consideration. It is worth noting that one of the customary objectives in selecting the value of the gate resistor is achieving high switching speed (for SiC or GaN unipolar devices this means high dV/dt during the Miller period), which requires a low gate resistor value. However, a low gate resistor value also reduces the damping ratio of the gate loop and increases the likelihood of instability.

The authors propose that a figure of merit useful to the application designer which takes this trade-off into consideration is the normalized gate resistance, which can be expressed as $\mathrm{R_{G_NORM}} = \mathrm{R_G}/\left[\sqrt{\mathrm{L_G}/\mathrm{C_2}}\right] = 2\zeta$, where ζ is the damping ratio of the gate loop, and C_2 is the gate-source capacitance of the transistor in question when the gate node is biased near threshold. The following figures illustrate the impact of the normalized gate resistance for both the special case without significant drain-source capacitance (Fig. 4) and the general case, which includes drain-source capacitance (Fig. 5). Each of these figures considers a range of normalized gate resistance values which is designed to simulate the configuration of a SiC half-bridge circuit set up for fast switching. It can be observed from these figures that the influence of a reduction in R_{G_NORM} is universally de-stabilizing, since the normalized conductance curves appear at more negative values for lower values of R_{G_NORM}. However, it can also be stated that the model is much more sensitive to the value of R_{G_NORM} for devices without significant drain-source capacitance. The reason for this difference can be attributed to the self-snubbing capability of devices which contain significant drain-source capacitance.

Another consideration worth mentioning in regard to the value of gate resistance in the context of half-bridge circuits is the possibility of shoot-through due to Miller turn-on of the inactive switch (Q_1). When a positive dV/dt is expressed across Q_1 during the turn-on of Q_2, displacement current flows through the Miller capacitor of Q_1 and must be sunk by the gate-drive circuit attached to this switch. If the displacement current cannot be absorbed quickly enough by the gate drive, the gate-source capacitance may charge up, and Q_1 will turn on if the gate potential rises to threshold. The traditional method for managing this behavior is to use a low gate resistor value to ensure a low-impedance connection between the FET gate node and the gate-drive circuit. This methodology is effective in managing Miller turn-on of the inactive switch, but also serves to reduce the effective damping of the gate-loop and can therefore exacerbate the instability problem.

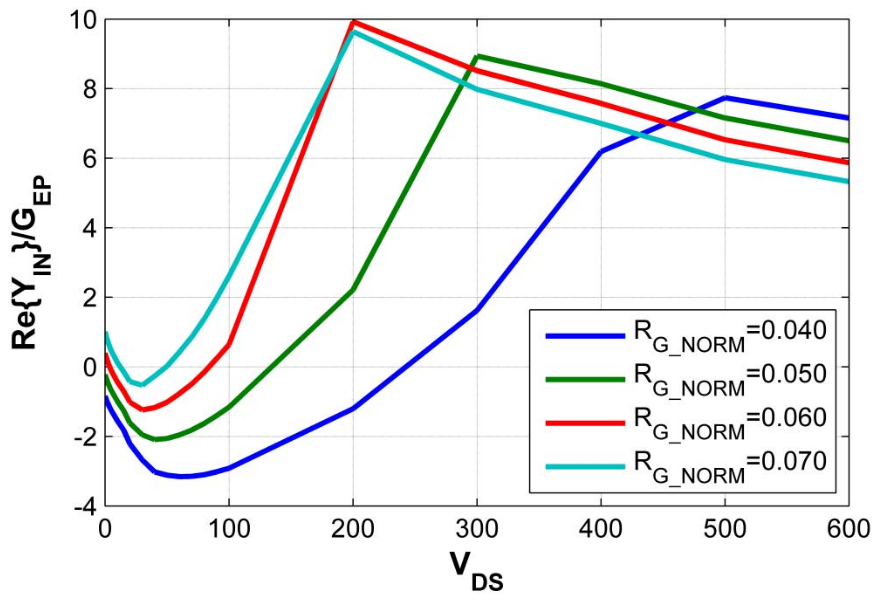

Fig. 4. Influence of normalized gate resistance on stability of exemplary SiC FET without significant drain-source capacitance

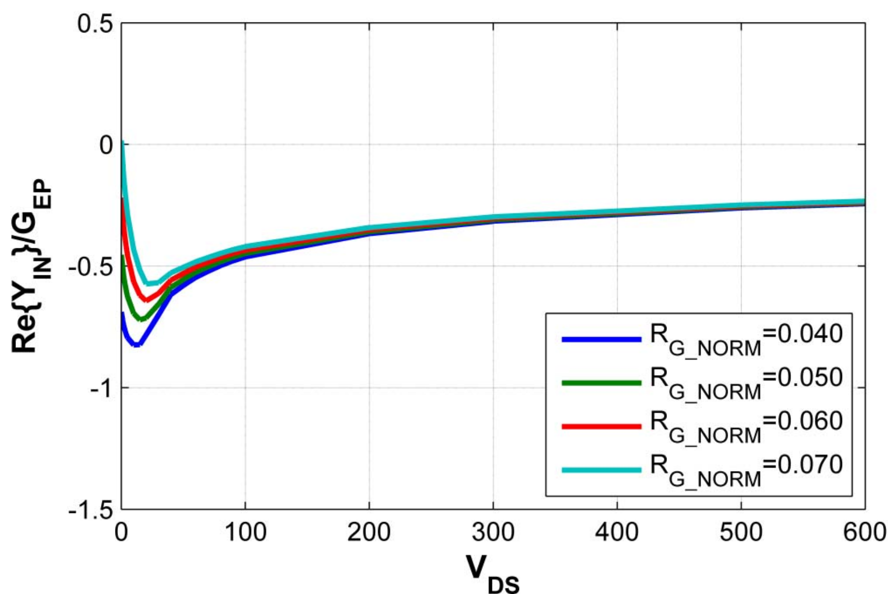

Fig. 5. Influence of normalized gate resistance on stability of exemplary SiC FET with fixed drain-source capacitance of 1 nF

3.2. Gate-Source Capacitance

The conflicting demands made on the gate-resistor value selection by switching speed, risk of instability, and risk of Miller turn-on suggest that a single degree of freedom is inadequate to simultaneously satisfy each of these requirements. An additional degree of freedom which is available to the circuit designer which may not be generally considered is the ability to augment the gate-source capacitance of the FET by adding an external linear capacitor across the gate and source terminals of the device. This methodology has been proposed in [3] as a means of simultaneously reducing the risk of Miller turn-on and the risk of FET instability. The addition of external gate-source capacitance is effective in reducing the risk of Miller turn on because it shifts the ratio of the capacitive divider present across the drain-gate-source nodes, as reflected by C_1 and C_2 in the small signal model of Fig. 3. Increasing the value of C_2 increases the threshold of displacement current required to cause the gate node to rise to threshold.

Furthermore, increasing the value of C_2 can also benefit the stability of the SiC FET half-bridge. This result is demonstrated by evaluation of the $Re\{Y_{IN}\}/G_{EP}$ ratio of the power oscillator small-signal model. Fig. 6 and Fig. 7 present an evaluation of this normalized conductance ratio parameterized by the value of an externally-applied gate-source capacitor. Fig. 6 applies to the special case of a device without significant drain-source capacitance; Fig. 7 applies to the general case of a device which incorporates drain-source capacitance.

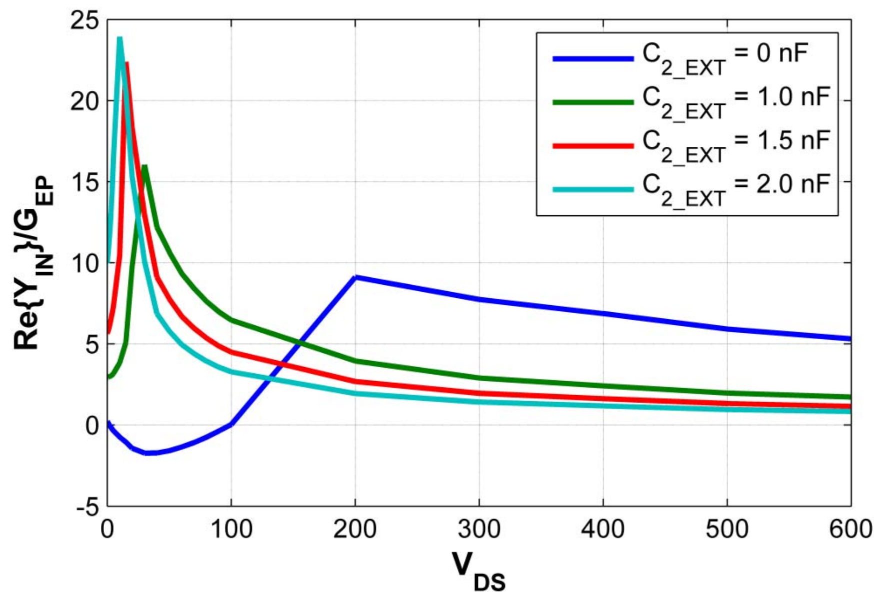

Fig. 6. Influence of addition of external gate-source capacitance to exemplary SiC FET without appreciable drain-source capacitance

In the special case of a device with negligible drain-source capacitance, the effect of adding external gate-source capacitance is found to have a significant effect on the stability of the associated system. This can be observed in Fig. 6 by comparing the C_{2_EXT}=0 curve with the C_{2_EXT}=1 nF curve, for example. The pseudo-quadratic portion of the C_{2_EXT}=0 curve which appears between 0 and 200 V is observed to be shifted for the C_{2_EXT}=1 nF curve. In this case, the quasi-quadratic is observed to be both translated to more positive conductance values and compressed toward a lower voltage range (0 – 30 V). Since this curve does not intersect the -1 point, this configuration is not expected to be subject to self-sustained oscillation. Further increases to the value of the external gate-source capacitor value are observed to continue this trend and provide additional stability margin.

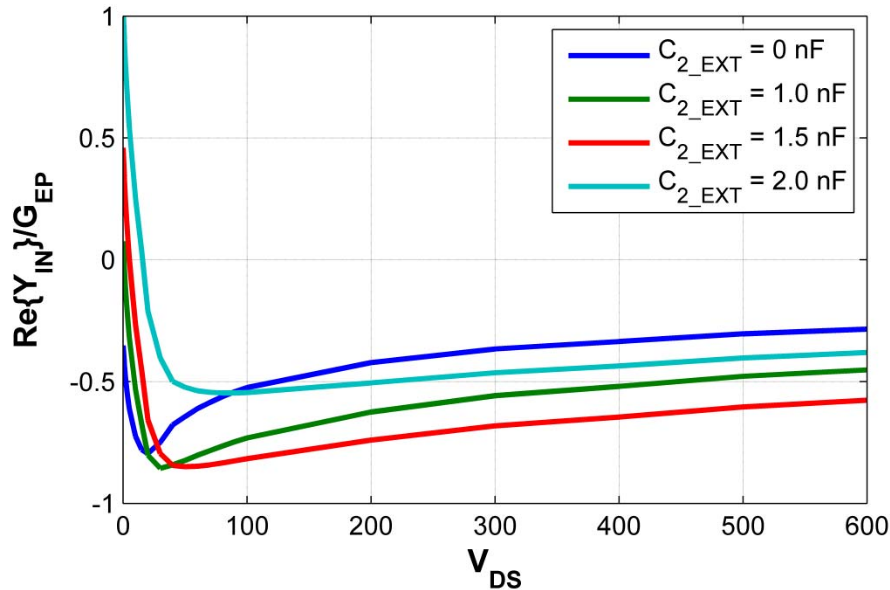

Fig. 7. Influence of addition of external gate-source capacitance to exemplary SiC FET with fixed drain-source capacitance of 1 nF

In the general case (Fig. 7), the relationship between the value of C_{2_EXT} and the susceptibility to self-sustained oscillation is more complex. For small values of C_{2_EXT} (e.g., 1 nF), the stability margin is actually reduced compared to the case with zero C_{2_EXT}. However, larger values of C_{2_EXT} are observed to push the conductance curves toward more positive values, thereby increasing the stability margin of the system. Although the exemplary circuit configuration represented by Fig. 7 does not demonstrate any conductance curves which indicate instability, it should not be assumed that all such circuits are immune from this phenomenon. Instability has been empirically observed by the authors in a half-bridge circuit corresponding to the general case represented here.

4. Methods for Mitigation

There are several strategies for mitigation of the self-sustained oscillation phenomenon which are known to be effective. As mentioned previously, the starting point for reducing the susceptibility to this phenomenon is the reduction of gate-loop parasitic inductance to the extent possible. While it is not possible to completely eliminate the aggregate gate-loop inductance, it has been shown that careful layout practices can significantly reduce the impact of parasitic gate-loop inductance and improve the stability margin of fast-switching circuits [5]. A second strategy for reducing susceptibility to this phenomenon is inclusion of this consideration in the process of gate resistor value selection. Use of a non-zero-valued gate resistor can provide significant damping of the gate-loop and provide a measure of protection against the occurrence of self-sustained oscillation. This strategy, however, carries with it two disadvantages: increased switching losses due to reduced switching speed and increased susceptibility to Miller turn-on. A third strategy which is not subject to this trade-off is the use of an external gate-source capacitor. This “ballasting” capacitor must be added very close to the FET die in order to prevent dilution of its effect by the influence of interconnect inductance. This approach provides protection against both the occurrence of instability and the occurrence of Miller turn-on, at the cost of an increase in maximum peak gate-drive current. A final approach which is being investigated by the authors is the use of a closed-loop gate-drive scheme based on a high-speed video op-amp [6]. The preliminary results of this study are promising, although it remains to be seen whether this strategy will be viable in the context of practical power electronics applications.

5. Conclusion

This paper has demonstrated the possibility of improper operation of SiC half-bridge circuits when the low intrinsic resistance and capacitance of these devices is not considered by application designers. These attractive properties of SiC devices give rise not only to the possibility of very fast switching and low-loss operation, but also to the possibility that circuits based on these devices will reveal undesirable resonant modes, including instability. This paper has described the phenomenon of half-bridge instability in the context of established negative oscillator design theory, and has provided a synopsis of practical methods which can be utilized to mitigate this behaviour when it is observed in application circuits.

6. Literature

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